LEVERAGING SERIAL DIGITAL INTERFACES STANDARDIZATION: THE RASTA REFERENCE ARCHITECTURE FACILITY AT ESA

Session: Spacewire onboard equipment and software

Short Paper

Aitor Viana Sanchez, Gianluca Furano, Massimiliano Ciccone, Farid Guettache, Claudio Monteleone, Chris Taylor

ESA - European Space Technology Centre (ESTEC)

ESA/ESTEC P.O. Box 299 / 2200AG Noordwijk ZH, the Netherlands

Manuel Prieto, Ignacio Garcia Tejedor

University of Alcala

Ctra. Madrid-Barcelona, km. 33.6, 28871 Alcala de Henares, Madrid

E-mail: aitor.viana.sanchez@esa.int, gianluca.furano@esa.int, massimiliano.ciccone@esa.int, farid.guettache@esa.int, claudio.monteleone@esa.int, chris.taylor@esa.int, manuel.prieto@aut.uah.es, ngarcia@aut.uah.es

ABSTRACT

This paper presents an overview of the internal R&D activity project in ESA called Reference Avionics System Test-bed Activity (RASTA). This activity aims to provide a hardware/software reference infrastructure where all the incoming TRP and GSTP activities can be integrated, coming out with a common testbed which may be missionized instead of dedicated environments for each activity.

Within RASTA, most of the space representative buses are included, CAN bus, MIL-STD-1553 and Spacewire. Several units comprise RASTA, such as: LEON2 based on-board computer, Telemetry and Telecommand control unit and a Mass Memory Unit, and the communication technology available so far may be selected between cPCI and Spacewire bus.

One of the latest activities started early this year is the Modular Advanced Mass Memory Architecture (MAMMA). This unit tends to be an *intelligent* unit fully based on Spacewire embedding several services being as autonomous as possible from the on board computer. This architecture will exploit the capabilities of active Spacewire backplanes.

Some RASTA building blocks for the space community are already available: Basic SW and SW drivers (CAN/1553/SpW, TT&C), OS abstraction layer, SW libraries (CFDP). In the future more SW libraries will be available (e.g. PUS library) and more HW units integrated in the environment (e.g. intelligent RTUs)

1 INTRODUCTION AND SCOPE

RASTA is a Data Systems Division's (TEC-ED) infrastructure for hosting, testing and validating hardware and software elements related to flight avionics. One of the main drivers for RASTA has been the need for an end-to-end reference system which can be used to integrate developments resulting from TRP and GSTP activities. RASTA objectives may be summarised as follows:

- To define an overall system that embodies the latest industrial agreements on avionics architectures and includes the necessary elements to cover the end-to-end communications associated with a typical spacecraft

- To provide a system with well defined software and hardware interfaces such that the modification/incorporation of new elements does not disturb the existing infrastructure

- To provide a specification of the reference system so that it may be applied to new developments and used for subsequent integration, test and evaluation

- To publicise the specifications for encouraging harmonisation within industrial infrastructures

- To utilise the system for project support in terms of mission design feasibility and performance

- To utilise the system for standards support including prototyping and validation of new protocols

- To evaluate the feasibility of new flight architectures, in terms of extended connectivity, functional redundancy, use of modern interfaces, use of rapid prototyping methods

- To enable connection with remote elements for example with ESOC ground related test-beds

To achieve its objectives, RASTA must therefore be completed with elements and functions that are in addition to the purely hardware aspects associated with flight avionics such as: an onboard basic software framework and ground developments (e.g. SCOS 2000).

The end-to-end RASTA configuration aims to be representative of a scenario where a Mission Control Centre (MCC) communicates to one or more spacecrafts through a TM/TC space link. Initially, in a configuration where more than one flight segment is present, only one flight segment is directly connected to the Ground System through a TM/TC link. All the additional Flight Segments will be interconnected trough a simulated inter-satellite link (i.e. Proximity-1) but not 'directly' reachable from the Ground Segment. In the near future it is foreseen to have a TM/TC link also to a second Flight Segment.

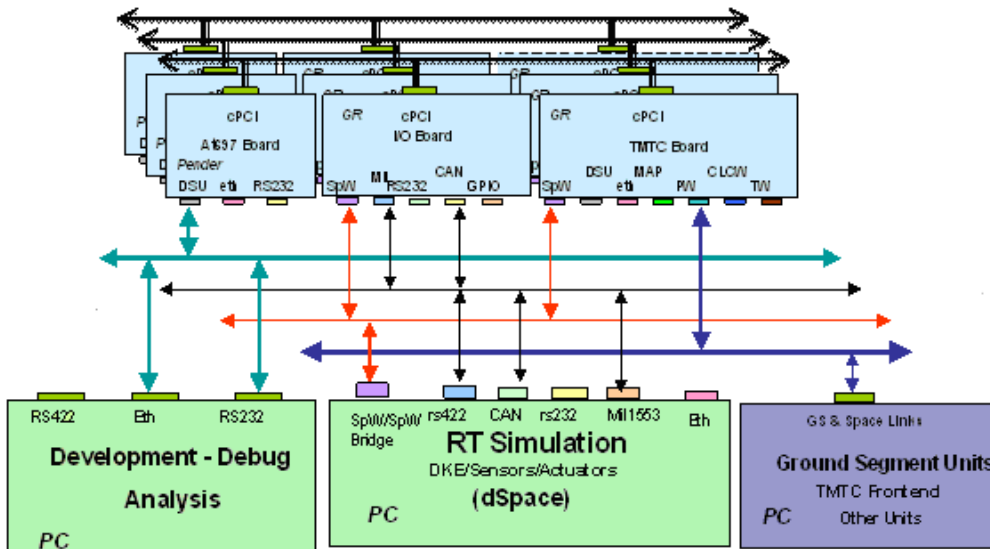Figure 1 represents a view of the main HW elements of RASTA and the way they interconnect.

Figure 1 - RASTA Hardware Overview

Several configurations may be tackled with RASTA, so far two configurations are considered. In the baseline configuration a ground segment is connected, through a simulated space link, to a single spacecraft made of two onboard computers (i.e. a CDMU and a Payload computer). While in the extended configuration the same ground segment is connected to two spacecrafts; respectively with two and one onboard computer (i.e. OBC 1 and OBC 2 as part of an orbiter. OBC 3 as part of a Rover). This two configurations will be used to cover various scenarios; from a simple one with a single spacecraft hosting a main OBC and a payload computer, to more complex one with 2 spacecrafts representing the combination of an orbiter and a lander or a lander and a rover.

In section 2.1 the hardware elements comprising RASTA will be detailed. In section 2.2, all the software building blocks available so far and the on-going ones will be briefly explained. The section 2.3, the parallel activity based on RASTA hardware dubbed MAMMA is explained. Finally, section 3 states the conclusions.

2   REFERENCE AVIONICS SYSTEM TED-BED ACTIVITY

2.1   RASTA HARDWARE

The Rasta hardware architecture is designed as an open system which provides physical framework to integrate components and subsystems, from the three domains described below, as they become available:

The On board data System

The on board data management product family is the core element of the facility. It is based on a generic repository of representative building blocks. It is composed of:

- Processor board, mainly LEON2/LEON3 Boards @ 100Mhz

- Interfaces to On board Communication system (Spacewire, CAN, Mil-Bus, RS422, RS232, Ethernet)

- Interfaces to TMTC (Packet-wire, MAP, CLTU)

These elements have been designed to be representative of flight hardware and to enable cross-coupling in FT architecture

The data system environment

The on board data systems environment consists mainly on AOCS/GNC related components and sub-systems (vehicle dynamics, kinetics, environment, sensors, actuators) and payload subsystem. These blocks can be either simulated on workstations or real units.

The ground equipment

Ground segment units representative of the real Ground Segment facility (TMTC Front End, etc...)

2.2 RASTA SOFTWARE

2.2.1 RTEMS REAL-TIME OPERATING SYSTEM

Real-Time Executive for Multiprocessor Systems is a free open source real-time operating system designed specifically for embedded systems. It is wide use for embedded applications and it is becoming a de-facto standard for space applications, mainly because the source code is fully available.

RTEMS has been designed to support different API standards (e.g. POSIX), also providing a native API and up to it RTEMS will be qualified.

RTEMS has been selected for being the RASTA RTOS mainly because it is open source, even though all the software assets for RASTA are mainly RTOS independent to ensure portability.

2.2.2 OPERATING SYSTEM ABSTRACTION LAYER (OSAL)

The goal of this library is to promote the creation of portable and reusable real time embedded software for RASTA. Given the necessary operating system abstraction layer implementations, the same embedded software might compile and run on different platforms and on a different operating system ranging from spacecraft computer systems to desktop PCs, ensuring that all the software deliverables for RASTA will work even when changing the platform, RTOS, etc.

The OSAL library is first coming from a NASA open source project ([1]), and has been adopted in RASTA to be one of the software cores of the system. TEC-EDD section at ESA is maintaining its own OSAL flavour and feed backing to NASA's project when a major change is performed.

2.2.3 CCSDS SPACECRAFT ON-BOARD INSTERFACE SERVICES (SOIS)

For the CCSDS SOIS ([4]), two independent activities are underway by SciSys (UK) and SAAB (S). Both activities take benefit from the sub network protocol prototyping activities for Milbus and Spacewire. The implementation from SciSys will use the OSAL abstraction library to ensure portability across different platforms and Operating Systems.

2.2.4 CCSDS FILE DELIVERY PROTOCOL (CFDP) LIBRARY

Within the RASTA activity, a CFDP ([2]) library together with a CFDP validation environment is being developed under a GSTP contract with SpaceBel. So far, the first deliverable comprising the validation environment and a CFDP library (non-flight version) is already available. A new flight version developed from scratch is on-going to be tested in RASTA.

2.3 RASTA RELATED ACTIVITIES

2.3.1 MODULAR ADVANCED MASS MEMORY ARCHITECTURE

This activity is framed into RASTA and will implement new development concepts for future Solid State Mass Memories (SSMM). MAMMA will be mainly based on space wire backplane connections between memory and MMU controller and, aims to be fully independent from the memory device technology while also focused on FLASH memories maximizing the performance over FLASH. To achieve that the memory access natively block-based, and any other access (e.g. byte based) is 'emulated' on top of it.

The activity is today half implemented using external SDRAM ([3]) memory connected to the controller using cPCI backplane. So far the maximum bandwidth achieved (write burst transfers, DMA, no EDAC) in this configuration is 70 Mbytes/s, which is the upper boundary. This data rate will for sure be lower when integrating the MMU communication protocol and using Spacewire as backplane. Some measurements have been already performed over the space wire interfaces in RASTA, to know exactly what bandwidth might be expected. Best effort tests over v (configured at 200 Mbps) in RASTA shows that only ~6 Mbytes/s data rate can be achieved (see Figure 2), and it is dependent from the packet size. Those numbers are reasonable having in mind the fact that Spacewire is implemented in RASTA using a 33 MHz FPGA.
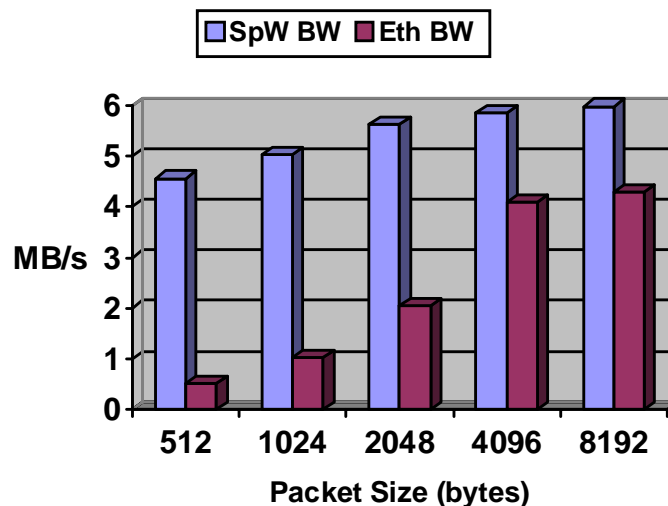

Figure 2 - RASTA SpW/Ethernet Bandwidth (Best Effort)

In the first half of the activity, the low level protocol to access the memory devices (local/remote access) and the error detection and correction mechanisms (RAID) have

been implemented and tested. From now until the end, the file system and the user communication protocol will be implemented and tested.

3 CONCLUSIONS

The paper shows how a « building block » approach in avionic systems prototyping and validation may lead to the development of innovative products and concepts that are of general space industry benefit.

The versatility of serial digital interfaces and the availability, for space systems of performance grades that until now were only possible with Commercial Of The Self based electronics allows also exploring new architectural concepts that increase failure tolerance and overall reliability of systems well beyond the simple cross strapped redundancy schemes used so far. The MAMMA Spacewire backplane powered mass memory here presented could be a good case of study.

4 REFERENCES

1. GSFC Open Source SW - http://opensource.gsfc.nasa.gov/projects/osal/osal.php

2. CSDS File Delivery Protocol (CFDP): Introduction and Overview. Green Book. Issue 3. April 2007

3. MM-6165D   2GB or 4GB 64-bit/66MHz PMC SDRAM Memory Buffer - http://www.vmetro.com/category4194.html

4. Spacecraft Onboard Interface Services. Green Book. Issue 1. June 2007 (http://public.ccsds.org/publications/SOIS.aspx)